ROHS Compliance, The RF MOSFET Line, Enhancement Mode

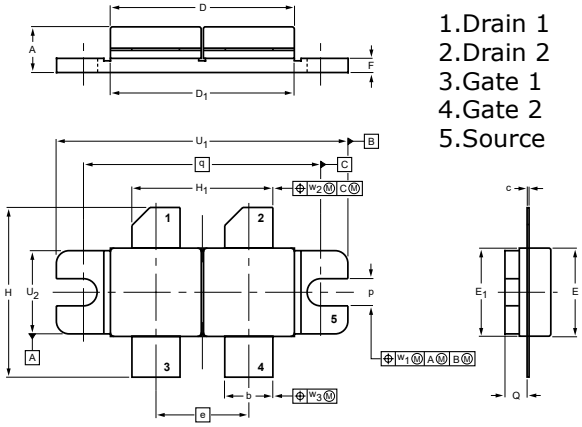
HG1020CN

Silicon MOS N-CHANNEL RF POWER TRANSISTOR

HG Semiconductors

DESCRIPTION

Silicon N-channel enhancement mode vertical D-MOS transistor is designed for 100MHz-500MHz



1.Drain 1
2.Drain 2
3.Gate 1
4.Gate 2
5.Source

FEATURES

- Output Power: 150 W
- Power Gain: 10 dB Min@400M, 28V
- Power Gain: 12.5 dB Typ@400M, 28V

DIMENSIONS

UNIT	A	b	c	D	D_1	e	E	E_1	F	H	H_1	p	Q	q	U_1	U_2	w_1	w_2	w_3
mm	5.77 5.00	5.85 5.58	0.16 0.10	22.17 21.46	21.98 21.71	11.05	10.27 10.05	10.29 10.03	1.78 1.52	21.08 19.56	17.02 16.51	3.28 3.02	2.85 2.59	27.94	34.17 33.90	9.91 9.65	0.25	0.51	0.25
inches	0.227 0.197	0.230 0.220	0.006 0.004	0.873 0.845	0.865 0.855	0.435	0.404 0.396	0.405 0.396	0.070 0.060	0.830 0.770	0.670 0.650	0.129 0.119	0.112 0.102	1.100	1.345 1.335	0.390 0.380	0.010	0.020	0.010

MAXIMUM RATINGS

CHARACTERISTICS	SYMBOL	RATINGS	UNITS
Drain–Source Voltage	V_{DSS}	70	V
Drain–Gate Voltage	V_{DGR}	70	V
Gate–Source Voltage	V_{GS}	±20	V
Drain Current — Continuous	I_D	26	A
Total Device Dissipation	P_D	400	W
Junction Temperature	T_J	200	°C
Storage Temperature Range	T_{STG}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX	UNITS
Drain–Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=100mA,V_{GS}=0	70	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS}=0V,V_{DS}=28V	-	-	5	mAdc
Gate–Source Leakage Current	I_{GSS}	V_{GS}=20V,V_{DS}=0V	-	-	1	uAdc
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = 10 V, I_D = 10mA	1.0	3.0	7.0	V
Forward Transconductance	gfs	V_{DS} = 10 V, I_D = 5A	4	-	-	S
Input Capacitance	Ciss	V_{DS} = 28 V,V_{GS} = 0 V, f = 1.0 MHz	-	-	320	pF
Output Capacitance	Coss		-	165	-	pF
Reverse Transfer Capacitance	Crss		-	15	-	pF
Common Source Power Gain	G_{PS}	V_{DD}=28V,P_{OUT}=150W, f=400MHz	10.0	12.5	-	dB
Drain Efficiency	η_D		50	55.0	-	%

Note : Above parameters , ratings , limits and conditions are subject to change.