HG Semiconductors

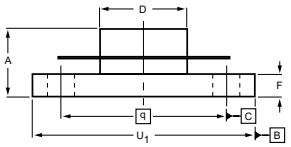
HG RF POWER TRANSISTOR

MRF171

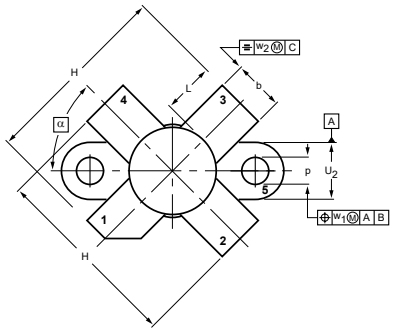
ROHS Compliance,Silicon NPN POWER TRANSISTOR

DESCRIPTION

Silicon N-channel enhancement mode vertical D-MOS transistor is designed use in 28 VdC large singal applications to 200 MHz



1.Collector
2.EMITTER
3.BASE
4.EMITTER
5.FIN



FEATURES

- Output Power: 45 W
- Power Gain: 12 dB Min@150M, 28V
- Efficiency: 50% Min

DIMENSIONS

NOTE: ALL ELECTRODES ARE ISOLATED FROM FLANCE.

UNIT	A	b	c	D	D_1	F	H	L	p	Q	q	U_1	U_2	U_3	w_1	w_2	α
mm	7.47 6.37	5.82 5.56	0.18 0.10	9.73 9.47	9.63 9.42	2.72 2.31	20.71 19.93	5.61 5.16	3.33 3.04	4.63 4.11	18.42	25.15 24.38	6.61 6.09	9.78 9.39	0.51	1.02	45°
inches	0.294 0.251	0.229 0.219	0.007 0.004	0.383 0.373	0.397 0.371	0.107 0.091	0.815 0.785	0.221 0.203	0.131 0.120	0.182 0.162	0.725	0.99 0.96	0.26 0.24	0.385 0.370	0.02	0.04	

MAXIMUM RATINGS

CHARACTERISTICS	SYMBOL	RATINGS	UNITS
Drain–Source Voltage	V_{DSS}	65	V
Drain–Gate Voltage	V_{DGR}	65	V
Gate–Source Voltage	V_{GS}	±40	V
Drain Current — Continuous	I_D	5	A
Total Device Dissipation	P_D	125	W
Junction Temperature	T_J	200	°C
Storage Temperature Range	T_{STG}	-65 to 150	°C

ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX	UNITS
Drain–Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=10mA,V_{GS}=0	65	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS}=0V,V_{DS}=28V	-	-	2	mA
Gate–Source Leakage Current	I_{GSS}	V_{GS}=40V,V_{DS}=0V	-	-	1	uA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = 10 V, I_D = 50mA	1.0	3.0	5.0	V
Forward Transconductance	gfs	V_{DS} = 10 V, I_D = 1A	1.2	1.8	-	mhos
Input Capacitance	Ciss	V_{DS} = 28V,V_{GS} = 0V, f = 1.0 MHz	-	140	-	pF
Output Capacitance	Coss		-	105	-	pF
Reverse Transfer Capacitance	Crss		-	10	-	pF
Common Source Power Gain	G_{PS}	V_{DD}=28V,P_{OUT}=45W, f=150MHz,I_{DQ}=30mA	12.0	15.0	-	dB
Collector Efficiency	η_C		50.0	60.0	-	%

Note : Above parameters , ratings , limits and conditions are subject to change.