HG Semiconductors

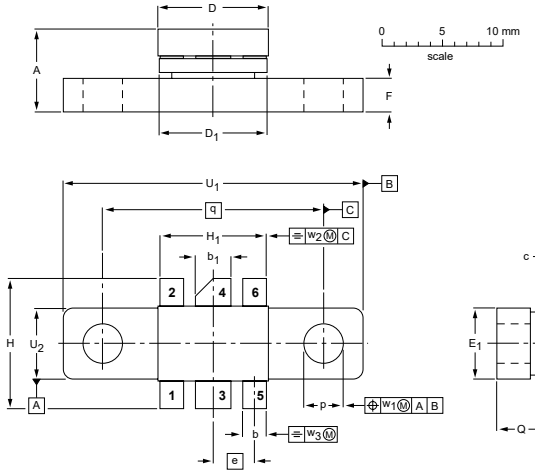
ROHS Compliance, The RF MOSFET Line, Enhancement Mode

MRF166C

Silicon MOS N-CHANNEL RF POWER TRANSISTOR

DESCRIPTION

Silicon N-channel enhancement mode vertical D-MOS transistor designed for large signal amplifier applications in the scope of 30-500Mhz



1.Source
2.Source
3.Gate
4.Drain
5.Source
6.Source
7.FIN

FEATURES

- Output Power: 20 W
- Power Gain: 17 dB Typ@400M, 28V
- Efficiency: 55% Typ

DIMENSIONS

UNIT	A	b	b_1	c	D	D_1	E	E_1	e	F	H	H_1	p	Q	q	U_1	U_2	w_1	w_2	w_3
mm	6.81 6.07	2.15 1.85	3.20 2.89	0.16 0.07	9.25 9.04	9.30 8.99	5.95 5.74	6.00 5.70	3.58	3.05 2.54	11.31 10.54	9.27 9.01	3.43 3.17	4.32 4.11	18.42	24.90 24.63	6.00 5.70	0.51	1.02	0.26
inches	0.268 0.239	0.085 0.073	0.126 0.114	0.006 0.003	0.364 0.356	0.366 0.354	0.234 0.226	0.236 0.224	0.140	0.120 0.100	0.445 0.415	0.365 0.355	0.135 0.125	0.170 0.162	0.725	0.980 0.970	0.236 0.224	0.02	0.04	0.01

MAXIMUM RATINGS

CHARACTERISTICS	SYMBOL	RATINGS	UNITS
Drain–Source Voltage	V_{DSS}	65	V
Gate–Source Voltage	V_{GS}	±40	V
Drain Current — Continuous	I_D	4	A
Total Device Dissipation	P_D	70	W
Junction Temperature	T_J	200	°C
Storage Temperature Range	T_{STG}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Drain–Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=5mA,V_{GS}=0	65	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS}=0V,V_{DS}=28V	-	-	1	mAdc
Gate–Source Leakage Current	I_{GSS}	V_{GS}=±40V,V_{DS}=0V	-	-	1	uAdc
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = 10 V, I_D = 25mA	1.0	-	6.0	V
Forward Transconductance	gfs	V_{DS} = 10 V, I_D = 1.5A	600	800	-	mhos
Input Capacitance	Ciss	V_{DS} = 28 V,V_{GS} = 0 V, f = 1.0 MHz	-	45	-	pF
Output Capacitance	Coss		-	38	-	pF
Reverse Transfer Capacitance	Crss		-	3.8	-	pF
Common Source Power Gain	G_P	V_{DD}=28V,P_{OUT}=20W, f=400MHz	14.0	17.0	-	dB
Drain Efficiency	η_D		50	55.0	-	%

Note : Above parameters , ratings , limits and conditions are subject to change.