

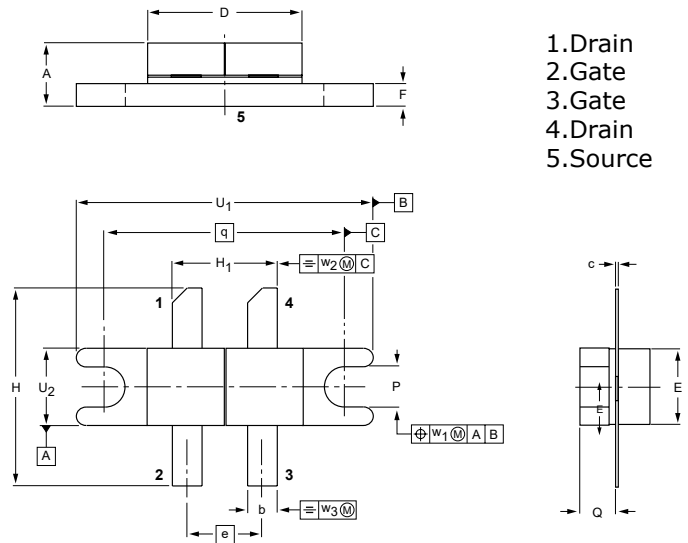
DESCRIPTION

Silicon N-channel enhancement mode vertical D-MOS transistor is designed for 1G PUSH-PULL applications.

FEATURES

- Output Power: 20W
- Power Gain: 10 dB Min@1G, 28V
- Efficiency: 40% Min

DIMENSIONS



UNIT	A	b	c	D	E	e	F	H	H ₁	p	Q	q	U ₁	U ₂	w ₁	w ₂	w ₃
mm	4.91 4.19	1.66 1.39	0.13 0.07	12.96 12.44	6.48 6.22	6.45	2.04 1.77	17.02 16.00	8.23 7.72	3.43 3.17	2.67 2.41	18.42	24.90 24.63	6.61 6.35	0.51	1.02	0.26
inches	0.193 0.165	0.065 0.055	0.005 0.003	0.510 0.490	0.255 0.245	0.254	0.080 0.070	0.670 0.630	0.324 0.304	0.135 0.125	0.105 0.095	0.725	0.980 0.970	0.260 0.250	0.02	0.04	0.01

MAXIMUM RATINGS

CHARACTERISTICS	SYMBOL	RATINGS	UNITS
Drain-Source Voltage	V _{DSS}	65	V
Gate-Source Voltage	V _{GS}	±20	V
Drain Current — Continuous	I _D	4	A
Total Device Dissipation	P _D	83	W
Junction Temperature	T _J	200	°C
Storage Temperature Range	T _{STG}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX	UNITS
Drain-Source Breakdown Voltage	V _{(BR)DSS}	I _D =10mA, V _{GS} =0	65	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} =0V, V _{DS} =28V	-	-	1	mAdc
Gate-Source Leakage Current	I _{GSS}	V _{GS} =20V, V _{DS} =0V	-	-	1	uAdc
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = 10 V, I _D = 10mA	1.0	-	7.0	V
Forward Transconductance	g _{fs}	V _{DS} = 10 V, I _D = 0.8 A	0.72	-	-	S
Input Capacitance	C _{iss}	V _{DS} = 28 V, V _{GS} = 0 V, f = 1.0 MHz	-	-	52	pF
Output Capacitance	C _{oss}		-	-	28	pF
Reverse Transfer Capacitance	C _{rss}		-	-	3	pF
Common Source Power Gain	G _{PS}	V _{DD} =28V, P _{OUT} =20W, f=1GHz	10.0	-	-	dB
Drain Efficiency	η _D		40	-	-	%
Load Mismatch Tolerance	VSWR		20:1	-	-	-

Note : Above parameters , ratings , limits and conditions are subject to change.