ROHS Compliance, The RF MOSFET Line, Enhancement Mode

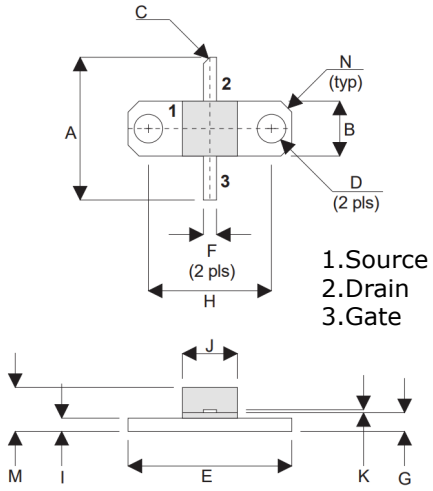
HG2005UK

Silicon MOS N-CHANNEL RF POWER TRANSISTOR

HG Semiconductors

DESCRIPTION

Silicon N-channel enhancement mode vertical D-MOS transistor is designed for 2G applications.



FEATURES

- Output Power: 7.5W
- Power Gain: 13 dB Min@1000M, 28V
- Efficiency: 40% Min

DIMENSIONS

DIM	mm	Tol.	Inches	Tol.
A	16.51	0.25	0.650	0.010
B	6.35	0.13	0.250	0.005
C	45°	5°	45°	5°
D	3.30	0.13	0.130	0.005
E	18.92	0.08	0.745	0.003
F	1.52	0.13	0.060	0.005

DIM	mm	Tol.	Inches	Tol.
G	2.16	0.13	0.085	0.005
H	14.22	0.08	0.560	0.003
I	1.52	0.13	0.060	0.005
J	6.35	0.13	0.250	0.005
K	0.13	0.03	0.005	0.001
M	5.08	0.51	0.200	0.020

MAXIMUM RATINGS

CHARACTERISTICS	SYMBOL	RATINGS	UNITS
Drain–Source Voltage	V_{DSS}	65	V
Gate–Source Voltage	V_{GS}	±20	V
Drain Current — Continuous	I_D	3	A
Total Device Dissipation	P_D	35	W
Junction Temperature	T_J	200	°C
Storage Temperature Range	T_{STG}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Drain–Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=10mA,V_{GS}=0	65	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS}=0V,V_{DS}=28V	-	-	2	mAdc
Gate–Source Leakage Current	I_{GSS}	V_{GS}=20V,V_{DS}=0V	-	-	1	uAdc
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = 10 V, I_D = 10mA	1.0	-	7.0	V
Forward Transconductance	gfs	V_{DS} = 10 V, I_D = 0.4A	0.54	-	-	S
Input Capacitance	Ciss	V_{DS} = 28 V,V_{GS} = 0 V, f = 1.0 MHz	-	-	39	pF
Output Capacitance	Coss		-	-	21	pF
Reverse Transfer Capacitance	Crss		-	-	2	pF
Common Source Power Gain	G_{PS}	V_{DD}=28V,P_{OUT}=7.5W, f=1000MHz	13.0	-	-	dB
Drain Efficiency	η_D		40	-	-	%
Load Mismatch Tolerance	VSWR		20:1	-	-	-

Note : Above parameters , ratings , limits and conditions are subject to change.