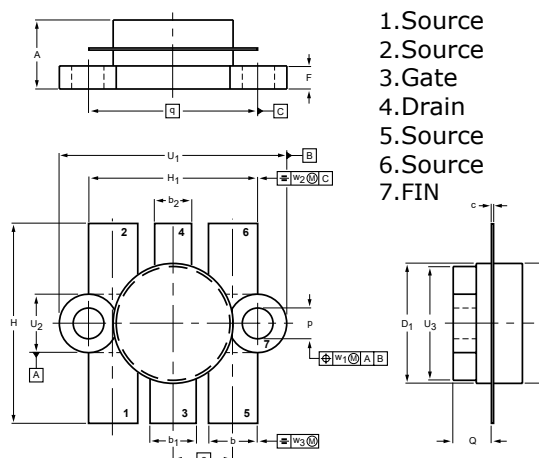


DESCRIPTION

Silicon N-channel enhancement mode vertical D-MOS transistor designed for large signal amplifier applications in the HF & VHF frequency range.

FEATURES

- Output Power: 60 W
- Power Gain: 16 dB Min@175M, 28V
- Efficiency: 50% Min



DIMENSIONS

NOTE: ALL ELECTRODES ARE ISOLATED FROM FLANGE.

UNIT	A	b	b ₁	b ₂	c	D	D ₁	e	F	H	H ₁	p	Q	q	U ₁	U ₂	U ₃	w ₁	w ₂	w ₃
mm	7.39 6.32	5.59 5.33	5.34 5.08	4.07 3.81	0.18 0.07	12.86 12.59	12.83 12.57	6.48	2.54 2.28	22.10 21.08	18.55 18.28	3.31 2.97	4.58 3.98	18.42	25.23 23.95	6.48 6.07	12.76 12.06	0.51	1.02	0.26
inches	0.291 0.249	0.220 0.210	0.210 0.200	0.160 0.150	0.007 0.003	0.505 0.496	0.505 0.495	0.255	0.100 0.090	0.870 0.830	0.730 0.720	0.130 0.117	0.180 0.157	0.725	0.993 0.943	0.255 0.239	0.502 0.475	0.02	0.04	0.01

MAXIMUM RATINGS

CHARACTERISTICS	SYMBOL	RATINGS	UNITS
Drain-Source Voltage	V _{DSS}	70	V
Gate-Source Voltage	V _{GS}	±20	V
Drain Current — Continuous	I _D	15	A
Total Device Dissipation	P _D	120	W
Junction Temperature	T _J	200	°C
Storage Temperature Range	T _{STG}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Drain-Source Breakdown Voltage	V _{(BR)DSS}	I _D =100mA, V _{GS} =0	70	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} =0V, V _{DS} =28V	-	-	1	mAdc
Gate-Source Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	1	uAdc
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = 10 V, I _D = 10mA	1.0	-	7.0	V
Forward Transconductance	g _{fs}	V _{DS} = 10 V, I _D = 3 A	2.4	-	-	mhos
Input Capacitance	C _{iss}	V _{DS} = 28 V, V _{GS} = 0 V, f = 1.0 MHz	-	185	-	pF
Output Capacitance	C _{oss}		-	95	-	pF
Reverse Transfer Capacitance	C _{rss}		-	7.5	-	pF
Common Source Power Gain	G _p		16.0	-	-	dB
Load Mismatch Tolerance	VSWR	V _{DD} =28V, P _{OUT} =60W, f=175MHz	20:1	-	-	-
Drain Efficiency	η _D		50	-	-	%

Note : Above parameters , ratings , limits and conditions are subject to change.