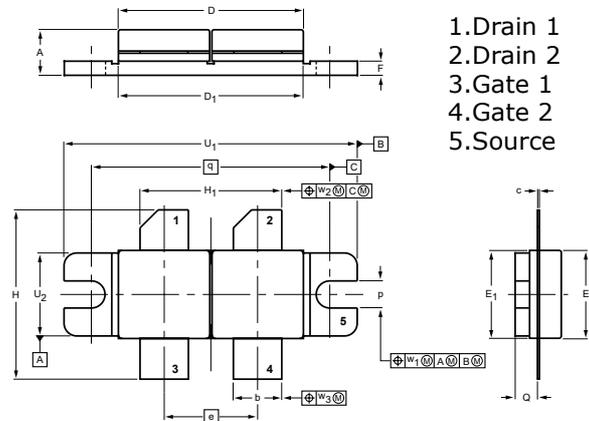


DESCRIPTION

Silicon N-channel enhancement mode vertical D-MOS transistor designed for large signal amplifier applications in the VHF frequency range.

FEATURES

- Output Power: 300 W
- Power Gain: 18 dB Typ@108M, 50V
14 dB Min@225M, 50V
- Efficiency: 80% Typ@108M, 50V
50% Min@225M, 50V



DIMENSIONS

UNIT	A	b	c	D	D ₁	e	E	E ₁	F	H	H ₁	p	Q	q	U ₁	U ₂	w ₁	w ₂	w ₃
mm	5.77 5.00	5.85 5.58	0.16 0.10	22.17 21.46	21.98 21.71	11.05	10.27 10.05	10.29 10.03	1.78 1.52	21.08 19.56	17.02 16.51	3.28 3.02	2.85 2.59	27.94	34.17 33.90	9.91 9.65	0.25	0.51	0.25
inches	0.227 0.197	0.230 0.220	0.006 0.004	0.873 0.845	0.865 0.855	0.435	0.404 0.396	0.405 0.396	0.070 0.060	0.830 0.770	0.670 0.650	0.129 0.119	0.112 0.102	1.100	1.345 1.335	0.390 0.380	0.010	0.020	0.010

MAXIMUM RATINGS

CHARACTERISTICS	SYMBOL	RATINGS	UNITS
Drain-Source Voltage	V _{DSS}	125	V
Gate-Source Voltage	±V _{GS}	20	V
Drain Current — Continuous	I _D	18	A
Total Device Dissipation	P _D	500	W
Junction Temperature	T _J	200	°C
Storage Temperature Range	T _{STG}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX	UNITS
Drain-Source Breakdown Voltage	V _{(BR)DSS}	I _D =50mA, V _{GS} =0	125	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} =0V, V _{DS} =50V	-	-	2.5	mAdc
Gate-Source Leakage Current	I _{GSS}	±V _{GS} =20V, V _{DS} =0V	-	-	1	uAdc
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = 10 V, I _D = 50mA	2.0	-	4.5	V
Forward Transconductance	g _{fs}	V _{DS} = 10 V, I _D = 5A	4.5	6.2	-	mhos
Input Capacitance	C _{iss}	V _{DS} = 50 V, V _{GS} = 0 V, f = 1.0 MHz	-	420	-	pF
Output Capacitance	C _{oss}		-	190	-	pF
Reverse Transfer Capacitance	C _{rss}		-	14	-	pF
Common Source Power Gain	G _{PS}	V _{DD} =50V, P _{OUT} =250W,	14.0	16.0	-	dB
Drain Efficiency	η _D	f=225MHz	50.0	55.0	-	%
Common Source Power Gain	G _{PS}	V _{DD} =50V, P _{OUT} =300W,	-	18.0	-	dB
Drain Efficiency	η _D	f=108MHz	-	80.0	-	%

Note : Above parameters , ratings , limits and conditions are subject to change.